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Characterization of scalable ion traps for quantum computation[1]
R.J. EPSTEIN, J.J. BOLLINGER, D. LEIBFRIED, S. SEIDELIN, J. BRITTON, J.H. WESENBERG, N. SHIGA, J.M. AMINI, R.B. BLAKESTAD, K.R. BROWN, J.P. HOME, W.M. ITANO, J.D. JOST, C. LANGER, R. OZERI, D.J. WINELAND, Time and Frequency Division, NIST, Boulder, Colorado 80305, USA — We discuss the experimental characterization of several scalable ion trap architectures for quantum information processing. We have developed an apparatus for testing planar ion trap chips [2,3], which features: a standardized chip carrier for ease of interchanging traps, a single-laser Raman cooling scheme, and photo-ionization loading of Mg^+ ions. The primary benchmark for a given trap is the heating rate of the ion motional degrees of freedom, which can reduce multi-ion quantum gate fidelities. As the heating rate depends on the ion trap geometry and materials, our testing apparatus allows for efficient iteration and optimization of trap parameters. With the recent ability to fabricate planar traps with sufficiently low heating rates for quantum computation [2], we describe current results on the simulation and fabrication of planar traps with multiple intersecting trapping zones for versatile ion choreography.

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[2]S. Seidelin *et al.*, Phys. Rev. Lett. **96**, 253003 (2006).
[3]J. Kim, *et al.*, Quantum Inf. Comput. **5**, 515 (2005).

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