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Atomistic pseudopotential simulation of nanometer sized CMOS devices[1] LIN-WANG WANG, Lawrence Berkeley National Laboratory, JUN-WEI LUO, SHU-SHEN LI, JIAN-BAI XIA, Institute of Semiconductors, Chinese Academy of Sciences — When the size of a CMOS is shrunk to 10-20 nm, quantum mechanical effects such as individual quantum levels, quantum tunneling, and single impurity fluctuations exhibit themselves. We have developed a method to calculate the electronic structures and I-V curves of million atom CMOS devices using atomistic pseudopotential method. The electronic structure is described by the empirical pseudopotentil. The Hamilotnian is solved using the linear combination of bulk band (LCBB) [1] method in which the electron wavefunction is expanded by a set of bulk Bloch functions. Approximated formulas are developed to describe the carrier occupation and the electron current in a source-drain biased nonequilibrium system. The electrostatic potential is calculated selconsistently by solving the Poisson equation with a given boundary condition and the occupied carried density. We will present the differences between the quantum mechanical results and the traditional semiclassical results in carrier charge density, electron current, turn-on gate potential and short channel effects. [1] L.W. Wang, A. Zunger, Phys. Rev. B 59, 15806 (1999).

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