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2D hole transport in GaAs MOSFETs TZU-MING LU, KEJI LAI, DANIEL TSUI, Princeton University, LOREN PFEIFFER, KEN WEST, Bell Laboratories, Lucent Technologies — We have fabricated enhancement-mode p-channel GaAs MOSFETs on the (100) surface of undoped GaAs/$Al_xGa_{1-x}As$ heterostructures, using atomic-layer-deposited Al_2O_3dielectric and Ti/Au gate, and measured their transport properties. The capacitively induced 2D hole density (p), determined from Shubnikov-de Haas oscillations, can be tuned from 9x$10^9$to 3x$10^{11}$$cm^{-2}$by applying a negative gate bias. Within this range, the effective capacitance is close to that of an ideal parallel plate capacitor, and the leakage current remains virtually zero. The highest possible density is limited by the heterostructure design, not by gate leakage. The 2D hole mobility at T=0.3K increases with p and saturates at 6.3x10^5 cm^2/Vs for p>2.3x$10^{11}$$cm^{-2}$. In this talk, we present data on transistor drain current-voltage characteristics, as well as magneto transport and the quantum Hall effects.

Tzu-Ming Lu
Princeton University

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