MAR07-2006-020259

Abstract for an Invited Paper
for the MAR07 Meeting of
the American Physical Society

Scalable Designs for Planar Ion Trap Arrays[1]

R.E. SLUSHER, Alcatel-Lucent

Recent progress in quantum operations with trapped ion qubits has been spectacular for qubit counts up to approximately ten ions. Two qubit quantum gates, quantum error correction, simple quantum algorithms and entanglement of up to 8 qubits have been demonstrated by groups including those at NIST, University of Michigan, University of Innsbruck and Oxford. Interesting problems in quantum information processing including quantum simulations of condensed matter systems and quantum repeaters for long distance quantum communication systems require hundreds or thousands of qubits. Initial designs for an ion trap "Quantum CCD" using spatially multiplexed planar ion traps[2] as well as initial experiments[3] using planar ion traps are promising routes to scaling up the number of trapped ions to more interesting levels. We describe designs[4] for planar ion traps fabricated using silicon VLSI techniques. This approach allows the control voltages required for the moving and positioning the ions in the array to be connected vertically through the silicon substrate to underlying CMOS electronics. We have developed techniques that allow the ion trap structures to be fabricated monolithically on top of the CMOS electronics. The planar traps have much weaker trapping depths than the more conventional multi-level traps. However, the trap depths are still adequate for trapping hot ions from many ion sources. The planar traps also involve more complex configurations for laser cooling and micromotion control. Initial solutions to these problems will be presented. Laser access to the ions can be provided by laser beams grazing the trap surface or by using vertical slots through the trap chip. We will also discuss limits imposed by power dissipation and ion transport through trap junctions (e.g. crosses and Ys). We have fabricated these VLSI based traps in a number of configurations. Initial fabrication and packaging challenges will be discussed.

[1]This research is supported by DTO. In collaboration with C. S. Pei, Y. L. Low, R. E. Frahm and H. R. McLellan,

[2]D. Kielpinski, C. Monroe, and D.J. Wineland, "Architecture for a large-scale ion-trap quantum computer," Nature, Vol.417, pp.709–711, (2002).

[3]S. Seidelin, J. Chiaverini, R. Reicle, J. J. Bollinger, D. Leibfried, J. Briton, J. H. Wesenberg, R. B. Blakestad, R. J. Epstein, D. B. Hume, J. D. Jost, C. Langer, R. Ozeri, N. Shiga, and D. J. Wineland, "Amicrofabricated surface-electrode ion trap for scalable quantum informtion processing," quant-ph/0601173, (2006).

[4]J. Kim, S. Pau, Z. Ma, H.R. McLellan, J.V. Gates, A. Kornblit, and R.E. Slusher, "System design for large-scale ion trap quantum information processor," Quantum Inf. Comput., Vol 5, pp 515–537, (2005).