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Novel Ferroelectric CMOS Circuits as a Nonvolatile Logic M. TAKAHASHI, T. HORIUCHI, Q.-H. LI, S. WANG, K. Y. YUN, S. SAKAI, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan — We propose a novel and promising nonvolatile-logic circuit constructed by p channel type (Pch) and n channel type (Nch) ferroelectric gate field effect transistors (FeFETs), which we named a ferroelectric CMOS (FeCMOS) circuit. The circuit works as both logic and memory. We fabricated a NOT logic FeCMOS device which have Pt metal gates and gate oxides of ferroelectric $SrBi_2Ta_2O_9$ (SBT) and high-k HfAlO on Si. Key technology was adjusting threshold voltages of the FeFETs as well as preparing those of high quality. We demonstrate basic operations of the NOT-logic response, memory writing, holding and non-destructive reading. The memory writing is done by amplifying the input node voltage to a higher level when the node was logically high and to a lower one when it was logically low just before the writing operation. The data retention was also measured. The retained high and low voltages were almost unchanged for 1.2 days. The idea of this FeCMOS will enhance flexibility of circuit designing by merging logic and memory functions.
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