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Study on threshold voltages of Pt/$SrBi_2Ta_2O_9$/Hf-Al-O/Si FeFETs Q.-H. LI, M. TAKAHASHI, S. WANG, T. HORIUCHI, C.C. WANG, K.Y. YUN, Y. FUHIHATA, S. SAKAI, National Institute of Advanced Industrial Science and Technology, Tsukuba, Japan — Complementary ferroelectric-gate field-effect transistors (FeFETs) are attractive for nonvolatile-logic circuit applications after the achievement of long data retention for both n- and p- channel FeFETs [1, 2]. To demonstrate nonvolatile logic circuits, the threshold voltage should be well controlled. Due to ferroelectricity two threshold voltages $V_{t,left}$ and $V_{t,right}$ can be defined from $I_d - V_g$ curves as gate voltages at I_d =10^{-6}A. More than 90 n- or p-channel Pt/$SrBi_2Ta_2O_9$/Hf-Al-O/Si FeFETs on a Si chip are studied. The average$V_{t,left}$ and $V_{t,right}$ are 1.19 and 2.38 V for n-channel FeFETs, and -0.76 and 0.40 V for p-channel FeFETs, respectively. The standard deviations of V_t are 3-5% and 7-8% of the memory window for the n- and p- channel FeFETs, respectively. V_t positions are adjusted by varying the well doping concentrations. Our results indicate possible circuit demonstration. This work was partially supported by NEDO.
[1] S. Sakai, et al, *IEEE Electron Devices Lett.*, **25**, 369(2004).
[2] Q.-H. Li, et al , *Appl. Phys. Lett.* **89**, 222910 (2006).

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