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Si nanomembranes with mixed crystal orientations[1] SHELLEY SCOTT, DEBORAH COTTRILL, DONALD SAVAGE, MAX LAGALLY, University of Wisconsin-Madison — Higher-carrier-mobility CMOS devices enhance processor speed. Carrier mobility can be optimized by fabricating mixed regions of Si(110) (high hole mobility) and Si(001) (high electron mobility) on a single substrate, so-called hybrid-orientation technology (HOT). We fabricate a mixed-crystal-orientation material using Si nanomembrane (SiNM) transfer and overgrowth. The top Si layer of SOI(110) is patterned with an array of holes and removed from its handle substrate, creating a Si(110)NM, which is then bonded to Si(001). We deposit Si over the structure with CVD, which is much faster on Si(001) than on Si(110), allowing planarization of the surface (i.e., hole filling), to produce a flat mesh of Si(001) and Si(110) regions. We characterize the mesh with XRD, SEM, and AFM. We can fabricate HOT membranes for transfer to various (including flexible) substrates, and can incorporate strain to tune mobilities. With strained Si(110)NMs, we expect a hole mobility enhancement of ∼70% over Si(001) while maintaining the high electron mobility of Si(001), thereby dramatically reducing the mobility imbalance between n and p-type devices.

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Shelley Scott
University of Wisconsin-Madison

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