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The Nanowire iJFET BART SOREE, WIM MAGNUS, IMEC, Kapeldreef 75, B-3001 Leuven, Belgium — The cylindrical geometry of nanowire surrounding gate MOSFETs gives rise to outstanding electrostatic control in comparison to planar devices. On the other hand, we expect that for ultrasmall nanowire diameters, the interaction of electrons with the surface (e.g. surface roughness and high-k) will be detrimental for device performance due to mobility degradation. In order to avoid these surface interactions we consider a surrounding gate nanowire operated not in MOSFET mode, but in "JFET mode." We thus consider a nanowire with silicon body radius R and surrounding oxide of thickness $t_{\rm ox}$ with a surrounding metal gate where both source, drain and silicon body are doped uniformly with a donor density $N_{\rm D}$. Applying a negative gate voltage pushes the electrons away from the interface between the insulator and metal gate, and as a result a depletion region is induced. For sufficient negative gate voltage the depletion region reaches the center of the silicon body, and pinch-off occurs. For large radii, we construct a compact model, and we show that reasonable pinch- off voltages are realized when the wire radius or the donor density is sufficiently small. Using the gradual channel approximation we are able to obtain current-voltage characteristics that constitute a "proof of concept" for this device. In the case of ultrasmall radii, we perform a quantum mechanical analysis of the electronic structure.

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