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III-V MOSFETs: From Materials & Physics to Devices

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Gallium-Arsenide metal-oxide-semiconductor field-effect-transistors (MOSFET) have finally been demonstrated with performance metrics matching the predictions of semiconductor device models. Recent discoveries and inventions in many areas including materials and fabrication, semiconductor physics, interface chemistry, semiconductor interface analysis, and semiconductor device design and process have contributed to this success. In my invited talk, I will review some select areas including the unique properties of interfaces formed between Ga_2O molecules and a GaAs surface, a high permittivity ($\kappa \cong 20$) $GdGaO/Ga_2O_3$ dielectric stack providing both a device quality interface and band-offsets on GaAs required for MOSFET operation, a semiconductor heterostructure for mitigation of high band-edge interface-state density, and device design criteria for high electron channel mobility and MOSFET drive current. Performance metrics of present metal-gate GaAs enhancement-mode MOSFETs such as electron channel mobility, drive current, transconductance, and threshold voltage will be discussed. GaAs MOSFETs with $In_{0.3}Ga_{0.7}As$ channel layers exhibit typical electron peak mobilities exceeding 5,000 cm^2/Vs, an improvement of a factor of 20 over silicon based high-κ metal-gate inversion-mode MOSFETs. Even higher electron mobilities surpassing 12,000 cm^2/Vs have been measured in $In_{0.75}Ga_{0.25}As$ channel layers. Beside the use of channel materials such as $In_xGa_{1-x}As$ with high bulk electron mobility, the physics of device operation is distinctively different from silicon inversion-mode MOSFETs. III-V MOSFET are now considered an option for CMOS based circuitry beyond the 22 nm node of the International Technology Roadmap for Semiconductors. High channel mobilities and the first successful implantation of III-V MOSFETs seem to justify such contemplation, however, many obstacles remain.