Abstract Submitted
for the MAR08 Meeting of
The American Physical Society

High Performance Silicon Nanowire Field Effect Transistor[1] QILIANG LI, Professor of Electrical Engineering, George Mason University, XIAOXIAO ZHU, YANG YANG, DIMITRIS IOANNOU, JOHN SUEHLE, CURT RICHTER — We report the fabrication and characterization of double-gated Si nanowire field effect transistors with excellent electrical characteristics and a small subthreshold slope: ∼ 85 mv/dec. The Si nanowires were grown by chemical vapor deposition at pre-defined location on a 50 nm thermal SiO_2 (bottom gate oxide). The source/drain electrodes (Al) were formed by using photolithographic alignment and metal lift-off processes. The nanowires were then covered with HfO_2 via atomic layer deposition. A thin layer of SiO_2 was deposited on the HfO_2 as a buffer layer before the top gate electrode formation (Al, using photolithographic and lift-off processes). This self-aligned process enables the integration of a large number of high-quality nanowire transistors for electronic circuitry. We have investigated the effect of device structure and annealing conditions on the final device performance, and developed theoretical models to assist the device optimization.

[1]We acknowledge the support of the NIST Office of Microelectronics Programs and Semiconductor Electronics Division.

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Date submitted: 27 Nov 2007 Electronic form version 1.4