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Interference of Electron Waves in a Ballistic Graphene Transistor.¹ SUNGJAE CHO, MICHAEL FUHRER — We have prepared singleand few-layer graphene samples by mechanical exfoliation of Kish graphite on SiO_2/Si substrates. We have fabricated graphene field-effect transistors by electron beam lithography followed by thermal evaporation of Cr/Au or Permalloy source and drain electrodes; the conducting silicon underneath 300 nm silicon dioxide serves as a back gate electrode. We find that at low temperatures that the two-dimensional plot of conductance as a function of gate voltage and drain voltage shows an interference pattern of maxima and minima which occur along diagonal lines. We analyze the pattern in terms of interference of electron waves reflected between source and drain electrodes. The slope of the lines measures the compressibility of the two-dimensional electron system, and has strikingly different dependence on carrier density (gate voltage) for single- and few-layer graphene samples, as expected theoretically.

¹Interference of Electron Waves in a Ballistic Graphene Transistor

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