Abstract Submitted
for the MAR09 Meeting of
The American Physical Society

Room-Temperature Single-Electron Transistors fabricated using CMOS-compatible processes VISHVA RAY, RAMKUMAR SUBRAMANIAN, PRADEEP BHADRACHALAM, SEONG JIN KOH, The University of Texas at Arlington — A critical requirement for the fabrication of single-electron devices is that the device components (Coulomb island, source, drain, and gate electrodes) be arranged with nanometer scale precision. We present a new single-electron device structure which consists of vertically stacked source and drain electrodes separated by a thin dielectric film. Using this configuration, we were able to control the gap between the electrodes with nanometer scale precision over an entire wafer, thereby allowing the concurrent fabrication of many device units in parallel processing. Coulomb islands (10 nm Au nanoparticles) were positioned in the gap between the source and the drain electrodes. Individually addressable gate electrodes were then incorporated in these devices, also in complete parallel processing. These devices have yielded clear single-electron transport characteristics (Coulomb blockade/staircase and Coulomb oscillations) at room temperature as well as at low temperatures ($\sim$10 K). The experimental data is in excellent agreement with the orthodox theory of single-electron tunneling. This study suggests that the fabrication of chip-level integrated systems of single-electron devices may now be possible using current CMOS fabrication technology. (ONR (N00014-05-1-0030), NSF CAREER (ECS-0449958), and THECB ARP (003656-0014-2006)).

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Date submitted: 20 Nov 2008 Electronic form version 1.4