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Optimizing Graphene Morphology on SiC(0001)

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Many schemes to integrate graphene with microelectronics assume that reliable wafer-scale synthesis processes will be developed. One promising route to wafer-scale synthesis is to form graphene overlayers from the decomposition of SiC at high temperature. We have shown that, even at 1200 C, limited diffusion at the SiC surface leads to pit formation and a non-uniform graphene film thickness [1]. In this talk I will describe our efforts to improve both graphene domain size and thickness uniformity. One way we achieve this is by forming graphene in a background pressure of disilane, which hinders SiC decomposition. Even in rather low Si partial pressures (e.g. 1e-5 Torr), the SiC decomposition temperature can shifted several hundred degrees higher in temperature [2]. Using in situ low-energy electron microscopy (LEEM), we show that this effect can be exploited to form large graphene domains (larger than 10 um) with controlled layer thickness (e.g. 1 ML). Work performed in collaboration with R.M. Tromp.

[1] J.B. Hannon and R.M. Tromp, Phys. Rev. B77, 241404(R) 2008
[2] R.M. Tromp and J.B. Hannon, in press.