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CMOS-analogous wafer-scale nanotube-on-insulator approach for submicron devices and integrated circuits using aligned nanotubes KOUNGMIN RYU, ALEXANDER BADMAEV, CHUAN WANG, CHONGWU ZHOU, University of Southern California — Massive aligned carbon nanotubes hold great potential but also face significant integration / assembly challenge for future beyond-silicon nanoelectronics. We report our recent advance on full wafer-scale processing of massively aligned carbon nanotube arrays for high performance submicron channel transistors and integrated nanotube circuits, including the following essential components. 1) The massively highly aligned nanotubes were successfully grown on 4 inch quartz and sapphire wafers via meticulous temperature control, and then transferred onto Si/SiO_2 wafers using our facile transfer printing method. 2) Wafer-scale device fabrication was performed on 4 inch Si/SiO_2 wafer to yield submicron channel transistors and circuits with high on-current density ~ 20 $\mu A/\mu m$ and good on/off ratio. 3) Chemical doping methods were successfully demonstrated to get CMOS inverters with a gain $\sim$5. 4) Defect-tolerant circuit design for NAND and NOR was proposed and demonstrated to guarantee the correct operation of logic circuit, regardless of the presence of mis-aligned or mis-positioned nanotubes.

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