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Ultralow thermal conductivity in Electrolessly Etched (EE) Silicon Nanowires¹ KEDAR HIPPALGAONKAR, RENKUN CHEN, BAIR BU-DAEV, Dept of Mech Eng, UC Berkeley, JINYAO TANG, SEAN ANDREWS, Dept of Chem, UC Berkeley, PADRAIG MURPHY, SUBROTO MUKERJEE, JOEL MOORE, Dept of Phys, UC Berkeley, PEIDONG YANG, Dept of Chem, UC Berkeley, ARUN MAJUMDAR, Dept of Mech Eng, UC Berkeley — EE process produces single-crystalline Silicon nanowires with rough walls. We use suspended structures to directly compute the heat transfer through single nanowires. Nanowires with diameters less than the mean free path of phonons impede transport by boundary scattering. The roughness acts as a secondary scattering mechanism to further reduce phonon transport. By controlling the amount of roughness it is possible to push limits to the extent that nanowire conductance close to quanta of thermal conductance, $\pi k_B^2 T/6\hbar$ is observed. Traditionally, the lower limit of conductivity is amorphous Silicon at 1 W/mK at room temperature. The measured conductivity of our nanostructures challenges even this amorphous limit pointing towards previously unstudied mechanisms of thermal resistance. We measure thermal conductivity of \sim 150nm diameter EE wires to be \sim 1 W/mK.

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