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Semiconducting nanowire devices in out-of-plane geometry. PRADEEP MANANDHAR, SAMUEL T. PICRAUX, Center for Integrated Nanotechnologies, Los Alamos National Laboratory — Semiconducting nanowires are attractive components in the field of nanoelectronics, photonic and sensing applications. Experiments with nanowires have usually been performed in planar geometry. Here, we demonstrate the fabrication of nanowire devices in out-of-plane geometry by taking advantage of inherent growth direction of nanowire using the vapor-liquid-solid (VLS) method. Highly epitaxial semiconducting nanowires are grown on doped Si (111) substrate from Au nanoparticle seeds assembled in e-beam lithography patterns. The directed assembly of Au nanoparticles is achieved by molecular recognition through silanization process, or electrophoretic assembly. The versatility of the VLS method allows the growth of a wide range of semiconducting nanowires with controlled *in-situ* doping. The post-growth processes include CVD of SiO_2 filler layer, chemical mechanical polishing and light etching of the SiO_2 layer to expose nanowire tips. Top metal contacts are then deposited for electrical characterization and sensing applications. We will present the results of the vertical nanowire device performance.

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