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Charge transport in graphene field effect transistors with ferroelectric gating[1]

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Recent experiments on ferroelectrically gated graphene field effect transistors (GFeFETs) open new opportunities for exploring new graphene physics and functionalities. The non-linear, hysteretic dielectric response of ferroelectrics introduces non-volatility in GFeFETs, which can be utilized for memory and data storage applications. Here, we present a comprehensive way in understanding and controlling ferroelectric gating in GFeFETs. We quantitatively characterize the hysteretic ferroelectric gating using the reference of an independent background doping (n_{back}) provided by normal dielectric gating. More importantly, we prove that n_{back} can be used to control the ferroelectric gating by uni-directionally shifting the hysteretic ferroelectric doping in graphene. Utilizing this electrostatic effect, we demonstrate symmetrical bit writing in graphene-ferroelectric FETs with resistance change over 500% and reproducible no-volatile switching over 10^5 cycles. In the quantum hall regime (2K and 9T), by controlling the polarization magnitude in the ferroelectric dielectric layer, we observe additional integer quantization steps besides the well-known $(N+1/2)e^2/h$ steps. We also explore the possibility to introduce ultra-high charge carrier doping in graphene by ferroelectric gating.

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