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## **Physical Requirements and Opportunities for Dense Optical Interconnects to Chips** DAVID MILLER, Stanford University

Electrical interconnects are running into severe problems, especially in density and energy dissipation. Such interconnect problems exist at all levels in electronic systems, even down to interconnects to and on chips. Optics can fundamentally avoid these problems but the technological requirements on devices are challenging [1]. As a baseline, optical devices would have to operate as fast as the electronics (e.g., on-chip clock rates will rise to 14 GHz according to the International Technology Roadmap for Semiconductors), and with no more energy. The energy per bit for electrical off-chip interconnects, such as on backplanes, is a few pJ/bit in current research, and on-chip global interconnects are 1 pJ/bit or lower, with possibilities for 100's of fJ/bit. Hence research targets for optics should be in the 100 fJ/bit range so that there is sufficient benefit. The device energy for optical output (e.g., for a laser or a modulator) should be 10's of fJ/bit since energy is required also for driver and receiver circuits and for clocking. Received energies would then be fJ's given reasonable optical losses. With photodetector capacitance of fF's the absorbed optical energy is enough to generate photodetector voltage swings of 1 V, thus eliminating the receiver voltage amplifiers and their power dissipation. Such devices are aggressive but not unphysical, and may require combinations of our best optical nanotechnologies, including nanoresonators, quantum wells and/or dots, and nanometallic and/or plasmonic field enhancements. Any and all such devices and technologies must be integrable with silicon CMOS, not only for cost and manufacturability, but also to obtain the necessary low device capacitances. Specific prospects in nanometallic enhanced detectors and in germanium quantum wells on silicon will also be discussed.

[1] D. A. B. Miller, "Device Requirements for Optical Interconnects to Silicon Chips," Proc. IEEE 97, 1166 - 1185 (2009)