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Improved Josephson Qubits incorporating Crystalline Silicon Dielectrics YUANFENG GAO, LEON MAURER, DAVID HOVER, UMESHKUMAR PATEL, ROBERT MCDERMOTT, UW-Madison, Dept. of Physics — Josephson junction phase qubits are a leading candidate for scalable quantum computing in the solid state. Their energy relaxation times are currently limited by microwave loss induced by a high density of two-level state (TLS) defects in the amorphous dielectric films of the circuit. It is expected that the integration of crystalline, defect-free dielectrics into the circuits will yield substantial improvements in qubit energy relaxation times. However, the epitaxial growth of a crystalline dielectric on a metal underlayer is a daunting challenge. Here we describe a novel approach in which the crystalline silicon nanomembrane of a Silicon-on-Insulator (SOI) wafer is used to form the junction shunt capacitor. The SOI wafer is thermocompression bonded to the device wafer. The handle and buried oxide layers of the SOI are then etched away, leaving the crystalline silicon layer for subsequent processing. We discuss device fabrication issues and present microwave transport data on lumped-element superconducting resonators incorporating the crystalline silicon.

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