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Effect of SiO_2 surface treatment on graphene transistors fabricated on Si:SiO_2 substrates using a lithography free process[1] PRASOON JOSHI, VIJAY TOUTAM, SRINIVAS TADIGADAPA, Department Of Electrical Engineering, Penn State University, ADAM NEAL, Department Of Electrical Engineering, Purdue University, HUMBERTO GUTIERREZ, Department Of Physics, Penn State University — Reversal of p-doping to n-doping and hysteresis effects in graphene transistors on Si:SiO_2 have been reported before. In this detailed experimental study, comparison is made between electronic transport characteristics of single graphene layer transistors where the SiO_2 is subjected to different surface treatments such as, exposure to O_2 plasma (1), passivation with hexamethlydisilazane (2) and baking at 300 $^\circ$C (3) in laboratory ambient prior to graphene exfoliation. Time constants for the reversal of p-doping in vacuum at 298K are found to be smaller for surface treatments (2) and (3) in comparison to (1). Hysteresis effects are also suppressed in graphene transistors made with surface treatments (2) and (3) . The hysteresis in samples made with surface treatment (1) can be reduced by vacuum annealing as has been suggested before. However, all lithography free samples show reduced hysteresis compared to already published results even in as-fabricated condition.

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