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Experimental Demonstration and Characterization of on-chip high speed graphene interconnects XIANGYU CHEN, DEJI AKINWANDE, Stanford University, KEONGJAE LEE, MIT, GAEL CLOSE, Zurich Research Laboratory, IBM Research, SHINICHI YASUDA, Toshiba, Japan, BIPUL PAUL, Toshiba America Research, SHINOBU FUJITA, Toshiba, Japan, JING KONG, MIT, H.-S. PHILIP WONG, Stanford University — Graphene has been considered as one of the most promising candidates for future interconnect technology. In spite of the promising theoretical predictions and DC characterization results about the excellent current-carrying capability of graphene nanoribbons, experimental demonstration and characterization of high speed signaling performance of graphene interconnects is still very limited. Here we present the first monolithic integration of graphene with commercial CMOS technology and the first experimental demonstration of on-chip graphene interconnects that operates above 1 GHz. We also studied the the dependence of high frequency performance on graphene interconnect physical dimensions. Important physical parameters like mean free path of graphene are extracted from experimental data. We compared our experimental results with previous theoretical predictions and gave experimental performance projection of on-chip graphene nanoribbon interconnects with linewidth smaller than 100nm.

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