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Effective Materials Properties of Interconnections in Industrial Microprocessor Designs MARY LANZEROTTI, Pacific Lutheran University, GIOVANNI FIORENZA, RICK RAND, IBM T J Watson Research Center — This talk presents a methodology to evaluate tradeoffs between technology and design to obtain the highest performance in industrial VLSI designs [1]. It is well known that the most significant circuitry constraint is that signals must arrive on time. Since the design cycle is time-consuming and complex, there is a need to migrate designs to future technology nodes to amortize design cost. However, models do not exist [1] to guide designers in their evaluation of whether migrated designs will operate successfully in a future technology or whether migrated designs will cause chip failure. There is therefore a need to evaluate the impact of design changes on performance. This talk evaluates this impact and describes it as an effective change in material properties of the design interconnections. Model estimates are compared with industrial microprocessor design data [1]. References [1] M. Y. Lanzerotti, G. Fiorenza, R. Rand, "Impact of interconnect length changes on effective materials properties (dielectric constant)," *Proc. Ninth International ACM Workshop on System-Level Interconnect Prediction (SLIP 2007)*, Austin, TX, USA, March 17-18, 2007. Online: http://www.informatik.uni-trier.de/~ley/db/conf/slip/slip2007.html, current as of 11-16-2010.

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