

Abstract Submitted
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Ferroelectric gating of CVD graphene devices¹ GUANGXIN NI, YI ZHENG, National University of Singapore, KUI YAO, Institute of Material Research and Engineering (IMRE), BARBAROS ÖZYILMAZ, National University of Singapore, DEPARTMENT OF PHYSICS, NATIONAL UNIVERSITY OF SINGAPORE, 2 SCIENCE DRIVE 3, SINGAPORE 117542 TEAM, NANOCORE, NATIONAL UNIVERSITY OF SINGAPORE, 4 ENGINEERING DRIVE 3, SINGAPORE 117576 TEAM, INSTITUTE OF MATERIAL RESEARCH AND ENGINEERING (IMRE), 3 RESEARCH LINK, SINGAPORE 117602 COLLABORATION, NUS GRADUATE SCHOOL FOR INTEGRATIVE SCIENCES AND ENGINEERING, SINGAPORE 117597 TEAM — The recent availability of large area graphene has opened up new possibility in graphene research. We will first discuss experiments, where graphene on the ferroelectric substrate PZT allows the fabrication graphene field effect transistors (GFETs) and graphene memory within ± 1 V operating voltage with maximum doping exceeding 10^{13} cm⁻². Ferroelectric substrates may also be of importance for large scale applications. Graphene's exceptional optical and mechanical properties make it suitable also for transparent conductors (TCs). While chemical doping has been proven to be an efficient approach to achieving ultra-low sheet resistance, some challenges remain. Here we propose an alternative way to obtain low sheet resistance of graphene using ferroelectric gating.

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