

Abstract Submitted
for the MAR11 Meeting of
The American Physical Society

Via fabrication process for epitaxial superconducting qubits JEFFREY KLINE, FABIO DA SILVA, MICHAEL VISSERS, DAVID WISBEY, MARTIN WEIDES, DAVID PAPPAS, NIST — Reducing the density of spurious two level systems (TLS) in the dielectric layers of superconducting qubits has been shown to improve performance. We aim to reduce TLS density in the Josephson junction tunnel barrier through the use of epitaxial materials. The investigation of some new material systems using a trilayer process wherein the base electrode, tunnel barrier, and top electrode are grown and subsequently patterned is problematic due to sidewall damage during the mesa etch. We apply the via fabrication process wherein the base electrode and wiring insulator layers are grown and patterned prior to tunnel barrier growth. The via process is compatible with a different set of electrode materials than the trilayer process and allows us to investigate the suitability of these materials for qubit applications. We present room temperature and low temperature data for Re/Al₂O₃/Re Josephson junctions fabricated using the via process.

Jeffrey Kline
NIST

Date submitted: 19 Nov 2010

Electronic form version 1.4