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Large scale atomic engineering of silicon (100) surfaces KAI LI, University of Maryland, PRADEEP NAMBOODIRI, SUMANTH CHIKKAMARANAHALLI, JOSEPH FU, RICHARD SILVER, National Institute of Standards and Technology, NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY COLLABORATION, UNIVERSITY OF MARYLAND, COLLEGE PARK COLLABORATION — Control of atomic morphology at the micrometer scale has been a long term challenge to enable atomically precise manufacturing. In this presentation we describe our method to pattern micrometer scale, ordered features on a Si surface with subsequent etch and high temperature processing. Following high temperature UHV processing, high quality atomically-ordered surfaces are imaged using atomic-resolution STM. A significant attribute of these surfaces is that the micrometer scale features evolve, but persist, allowing external location of nanometer scale features as well as comprehensive control of atomic terrace sizes and step bunching. A multi step thermal process is used, resulting in surface with symmetric, reproducible step-terrace patterns and very wide atomically flat regions. A kinetic Monte Carlo (KMC) model is used to simulate the current induced electromigration process which is primarily responsible for the long range evolution of surfaces.

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