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### **Bonding principles of the Passivation Mechanism at III-V – oxide Interfaces**

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It has always been much more difficult to make FETs from GaAs than Si, because of ‘Fermi level pinning’ and the difficulty of passivating its surfaces and interfaces. These issues have been discussed from the early days of PCSI by Spicer et al [1] with their “unified defect model.” Hasegawa [2] introduced the idea of “Disorder Induced Gap states” (DIGS). Since 1997 it has been possible to make inverted MOSFETs on GaAs using the epitaxial Gadolinium gallium oxide [3], but the main impetus has been since 2003 to use atomic layer deposition to make scalable FETs, as recently achieved by Intel [4]. The obvious question is why GaAs is so much more difficult to passivate than Si. The early answer was that the native oxide was poor. But since the advent of good deposited ALD oxides on Si such as HfO<sub>2</sub> or Al<sub>2</sub>O<sub>3</sub>, this answer is no good, as they should also work on GaAs. They do to an extent, but the interfacial density of states is still too large and the CV plots are distorted. The cause of the defects is cannot be due to stress. The reason must be some underlying chemical reason. I show that the reason is the polar nature of bonding in GaAs and other III-Vs, and the driving force to keep the Fermi level in a gap. The electron counting rule of Pashley [5] that describes surface reconstruction is shown to be a variant of auto-compensation, and it is proposed to work more generally, at each layer deposition or growth on GaAs [6]. This leads to a continuous generation of defects if it is not satisfied. So the answer is to deposit oxide layers that meet this rule, and also break up any surface reconstructions that would lead to As-As dimers [6].

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