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Directions in High-k Gate Stacks: From Silicon Chips to Carbon Nanomaterials

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The successful implementation of high-k/metal gates for silicon CMOS has culminated a decade of research on metal-oxide interactions with silicon. The ability to profile materials on a nanometer length scale has greatly assisted our ability to tailor electrical properties to create functional devices. Initial concerns addressed with composition profiling (e.g. Si content, Hf diffusion, thermal stability) have been replaced by more advanced questions. For example, gate-first technologies often use threshold-modifying layers, whose electrical properties are closely linked with their depth distribution. Oxygen diffusion is another complex problem of current concern, where physical characterization by isotopic tracing has given valuable insights. A similar set of challenges will confront us in creating carbon-based devices. Much effort is focused on nucleation of dielectrics, along with stability and interactions with the channel. This parallels work in the early development of high-k/Si. This talk will review some important lessons from the past decade, and discuss how we can apply this knowledge to creating improved graphene-channel devices.