MAR12-2011-002935

Abstract for an Invited Paper
for the MAR12 Meeting of
the American Physical Society

Pushing the material limit and physics novelty in high κ's/high carrier mobility semiconductors for post Si CMOS

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The semiconductor industry is now facing unprecedented materials/physics challenges due to the scaling-limitation of Si CMOS transistor arising from non-scaling of matters, namely gate dielectrics and channel mobility. The new technology using high-κ plus metal gate on high carrier mobility semiconductors of InGaAs and Ge will lead to faster speed at lower power. The tasks for realizing the new devices equivalent oxide thickness (EOT) < 1 nm, interfacial density of state (D_{it}) $\leq 10^{11}$ $eV^{-1}cm^{-2}$, self-aligned process, low parasitic, and integration with Si, have been solved or are being feverishly studied. The key of achieving the above goals is to understand/tailor interfaces of the high κ's/InGaAs (Ge). Tremendous progress has been made using molecular beam epitaxy (MBE) and atomic layer deposition (ALD) high κ's of $Ga_2O_3(Gd_2O_3)$, Al_2O_3, and HfO_2, and the novel ALD/MBE dual dielectrics in attaining an EOT of 0.5 nm, D_{it} of low 10^{11} $eV^{-1}cm^{-2}$(with a flat D_{it} distribution versus energy), and thermal stability at high temperatures higher than 800°C of the MOS structures. Electronic/electrical characteristics of the hetero-structures have been studied using in-situ synchrotron radiation photoemission, cross-sectional scanning tunneling spectroscopy, capacitance (conductance)-voltage under various temperatures, and charge pumping methods. Device performance in world-record drain currents, transconductances, sub-threshold swings, etc. in self-aligned inversion-channel high κ's/InGaAs and /Ge MOSFET's will also be presented. This work has been supported by Nano National Program (NSC 100-2120-M-007-010) of the NSC of Taiwan, and the AOARD of the US Air Force.

In collaboration with J. Kwo, W. C. Lee, M. L. Huang, T. D. Lin, Y. C. Chang, Y. H. Chang, C. A. Lin, Y. M. Chang (NTHU and NTU in Taiwan), T. W. Pi, C. H. Hsu (NSRRC in Taiwan), Y. P. Chiu (NSYSU in Taiwan), C. Merckling (IMEC in Belgium), J. I. Chyi (NCU, Taiwan), and G. J. Brown (AFRL, USA).