MAR12-2011-002979

Abstract for an Invited Paper
for the MAR12 Meeting of
the American Physical Society

Exploring Ge and III-V devices to scale CMOS beyond the Si roadmap

MARC HEYNS, imec

There is lots of interest in the use of germanium and III-V compounds as channel material in future CMOS generations. Direct growth of Ge and III-V in Si trenches allows to co-integrate these materials on bulk Si substrates. The formation of antiphase domain boundaries during epitaxy of III-V materials can be avoided by creating double atomic steps at the bottom of the trench through controlled Ge surface profiling. Much effort was dedicated to the electrical passivation of the interface between the high-k dielectric and these materials. Despite its relatively poor stability GeO2-like passivation of Ge has been demonstrated for both pMOS and nMOS devices. Si capping layers of only a few monolayers were used to fabricate short channel Ge pMOS devices with high drive currents. Other successful Ge passivation methods are based on surface treatments such as in situ H2S or wet (NH4)2S. Devices in III-V materials often suffer from Fermi level pinning associated with a high density of defect states near the high-k/III-V interface. These defects can be suppressed by optimized (in-situ) surface treatments and precise control of the oxidation states at the high-k/III-V interface. The Al2O3/ InGaAs interface has been extensively investigated, often concentrating on the possibility to remove Ga and As oxides by exposure to trimethylaluminum (TMA) during atomic layer deposition (ALD), but good passivation has also been demonstrated with various other high-k materials. Since most III-V materials have a low conduction band density of states, the surface potential travels far into the conduction band before the necessary amount of mobile charge is accumulated at the interface. Therefore, the defect density at these energy levels must also be reduced, including border traps in the high-k layer that cause frequency dispersion in the capacitance-voltage behaviour. Finally, it is noteworthy to mention that the introduction of these advanced materials also allows the development of new device concepts, such as Implant-Free Quantum Well devices, heterojunction TunnelFETs and nanowire devices, that can fully exploit the properties of these new materials.