MAR12-2011-003806

Abstract for an Invited Paper
for the MAR12 Meeting of
the American Physical Society

**Electrical characterization of interfacial defects**

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Aggressive transistor scaling to achieve better chip functionality calls for the introduction of new dielectric and metal materials into traditional device gate stacks. The advanced gate stacks represent multilayer structures, the materials of which may strongly interact (primarily during high temperature processing), generating structural defects in these layers. These complex structures pose new challenges in interpreting electrical measurements, which are sensitive to even extremely small concentrations of electrically active defects. The critical task is, thus, to link the structural and electrical characteristics of these multicomponent gate stacks in order to identify and control defects affecting device performance. In this presentation, we focus on analyzing interfacial defects affecting electrical characteristics of the metal/high-k (HK) gate stacks, which are of major interest to the semiconductor industry. We first developed models of the physical processes governing the measurements of the electrical techniques we used that allowed us to extract the structural parameters of the defects from the electrical data. By comparing the extracted parameters to those obtained by ab initio calculations of the material structures, we identified the nature of the contributing defects. A recently proposed model for random telegraph noise (RTN) and frequency-dependent charge pumping (CP) measurements that takes into consideration the multi-phonon lattice relaxation induced by charge trapping/detrapping at the defect sites was employed to extract characteristics of the traps in the interfacial SiO2 layer in HfO2-based HK devices. Our results indicate that the electron capture/emission times are controlled by the lattice re-arrangement (caused by the trapped electrons) rather than by electron tunneling to/from the trap as generally assumed. The strong dependency of the measured values on defect relaxation and ionization energies allows these values to be extracted; the values can then be used as a defect identifier. Complementary modeling of the gate leakage current in HK devices during electrical stress using the same approach yields characteristics of the traps in the interfacial SiO2 layer contributing to trap-assisted tunneling (TAT). Based on the values obtained by RTN, CP, and TAT measurements, the electrically active defects were tentatively assigned to oxygen vacancies in various charged states. In all cases, stress-induced traps were generated exclusively in the interfacial layer of the HK stacks, consistent with earlier findings that HK dielectrics are more resistant to defect generation than SiO2. Based on these findings, as well as an earlier TEM/EELS study of the elemental composition of the breakdown path, we proposed that the breakdown path formation/evolution in the interfacial layer is associated with the growth of an oxygen-deficient filament facilitated by the grain boundaries in the overlaying high-k film. This model successfully describes the temperature-dependent evolution of interfacial layer degradation through various breakdown phases.