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Abstract for an Invited Paper
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Towards a scalable superconducting qubit architecture

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I will review IBM's current approach towards building a scalable superconducting qubit architecture. The goal is to build a system using quantum error correction schemes based on two-dimensional surface codes, which are predicted to have a remarkably low fault tolerant threshold. I will briefly outline the particular skew-square lattice configuration and describe the concept of logical qubits and gates. On the experimental side, I will show recent advances towards implementing such surface code. This includes improvements in qubit coherence times, now exceeding T1=5us reliably, achieved by shielding the sample from infrared radiation confirming other recent results. Additional approaches leading to even longer coherence times are reviewed. With improved coherence times we show improved gate fidelities of two-qubit gates based the cross-resonance effect – an all microwave approach towards implementing two-qubit gates. I will conclude by reviewing some interesting future engineering challenges that should be addressed on our way towards building a quantum computer.