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A general approach for high yield fabrication of CMOS compatible all semiconducting carbon nanotube field effect transistor MUHAMMAD R. ISLAM, KRISTY KORMONDY, ELIOT SILBAR, SAIFUL KHONDAKER, Nanoscience Technology Center, Department of Physics, University of Central Florida, Orlando, Florida — We report strategies of achieving both high assembly yield of carbon nanotubes at selected position of the circuit via dielectrophoresis (DEP) and field effect transistor (FET) yield using semiconducting enriched single walled carbon nanotube (s-SWNT) aqueous solution. When the DEP parameters were optimized for the assembly of individual s-SWNT, 97% of the devices show FET behavior with a maximum mobility of 210 cm^2/Vs, on-off current ratio $\sim 10^6$ and on conductance up to 3 μS, however with an assembly yield of only 33%. As the DEP parameters were optimized so that 1-5 s-SWNTs are connected per electrode pair, the assembly yield was almost 90% with $\sim$ 90% of these assembled devices demonstrating FET behavior. Further optimization gives an assembly yield of 100% with up to 10 SWNT/site, however with a reduced FET yield of 59%. Improved FET performance including higher current on–off ratio and high switching speed were obtained by integrating a local Al_2O_3 gate to the device. Our 90% FET with 90% assembly yield is the highest reported so far for carbon nanotube devices. Our study provides a pathway which could become a general approach for the high yield fabrication of CMOS compatible carbon nanotube FETs.

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