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Gate-Controlled P-I-N Junction Switching Device with Graphene Nanoribbon SHU NAKAHARAI, TOMOHIKO IIJIMA, SHINICHI OGAWA, National Institute of Advanced Industrial Science and Technology, HISAO MIYAZAKI, SONGLIN LI, KAZUHITO TSUKAGOSHI, National Institute for Materials Science, SHINTARO SATO, NAOKI YOKOYAMA, National Institute of Advanced Industrial Science and Technology — The concept of a novel graphene P-I-N junction switching device with a nanoribbon is proposed, and its basic operation is demonstrated in an experiment. The concept aims to optimize the operation scheme for graphene transistors toward a superior on-off property. The device has two bulk graphene regions where the carrier type is electrostatically controlled by a top-gate, and these two regions are separated by a nanoribbon which works as insulator. As a result, the device forms a (P or N)-I-(P or N) junction. The off state is obtained by lifting the band of the bulk graphene of the source side and lowering that of the drain side, so that the device forms a P-I-N junction. In this configuration, the leakage current is reduced more effectively than the conventional single gate transistors due to a high barrier height and a long tunneling length in the nanoribbon. The on state is obtained by flipping the polarity of the bias of either top-gate to form a P-I-P or N-I-N junction. An experiment showed that the drain current was suppressed in the cases of P-I-N and N-I-P compared to P-I-P and N-I-N, and all of the behaviors were consistent with what was expected from the device operation model. This research is granted by JSPS through FIRST Program initiated by CSTP.

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