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Delay Analysis of Graphene Field Effect Transistors and T-Gate Self-Aligned GFETs[1] HAN WANG, ALLEN HSU, KI KANG KIM, JING KONG, TOMAS PALACIOS, Massachusetts Institute of Technology — In this paper, we propose a new method for extracting the carrier transit delays in radio-frequency (RF) graphene field effect transistors (GFETs). This delay analysis not only gives deep physical insight into the carrier transport in the channel, but also provides valuable information that can guide the device engineers in optimizing the design of high performance RF GFETs. The contribution of this work is three-fold. First, GFETs are fabricated on sapphire substrate to reduce the parasitics from the GSG pads. This minimizes the error in measuring the S-parameter of the device and allows small-signal capacitances to be accurately extracted. Second, we present for the first time a detailed delay analysis of high frequency graphene transistors. Lastly, the simple and robust method proposed can accurately extract the intrinsic transit delay of the GFETs - the delay purely associated with the carrier transiting across the intrinsic gate region – and allows a new method for direct experimental extraction of the average carrier velocity in the channel. Based on the analysis, we propose a self-aligned device structure to minimize the parasitic delays in GFETs. This GFET structure uses a T-shape gate as the mask to allow the source and drain metals to be aligned to the edge of the gate. A T-gate self-aligned GFET with gate head of 300 nm and foot 50 nm is fabricated and its DC and RF characteristics are reported.

Han Wang
Massachusetts Institute of Technology

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