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Drain Current Saturation in Sub- μm Graphene Field Effect Transistors SHU-JEN HAN, IBM TJ Watson Research Center, DHARMENDAR PALLE, IBM Research Labs, Austin, AARON FRANKLIN, ALBERTO VLADES-GARCIA, IBM TJ Watson Research Center — Recently, graphene field-effect transistors (FET) with high cut-off frequencies (f_T) were reported; however, the devices showed very weak drain current saturation, leading to an undesirably high output conductance. A crucial figure-of-merit for analog/RF transistors is the intrinsic gain (gm/gds). In this work, we show that by employing an embedded gate structure with an equivalent oxide thickness less than 2 nm, strong drain current saturation can be obtained for graphene FETs with short channels. The mechanism was not entirely due to velocity saturation, but rather the combination of a shift of the Dirac point in the voltage domain and a strong bias-dependent gate capacitance. The mechanisms are also verified with models.

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