

MAR12-2011-020061

Abstract for an Invited Paper  
for the MAR12 Meeting of  
the American Physical Society

### **Charge Traps at and near High-K Oxide/III-V Interfaces<sup>1</sup>**

PAUL MCINTYRE, Stanford University

The effort to achieve higher performance metal-oxide-semiconductor (MOS) devices prompts interest in new semiconductor channel materials such as indium gallium arsenide that can achieve larger drive currents than state-of-the-art Si field effect transistors, at low operating voltages. In order for InGaAs-channel transistors to approach their performance limits, however, high permittivity (high-k) metal oxide gate dielectrics must be prepared on the III-V surface in a manner that produces a minimal areal density of charge-trapping defects. This presentation will review different experimental approaches to prepare relatively passive interfaces between deposited oxides and GaAs or InGaAs. Both pre-oxide deposition and post-deposition methods will be summarized. It will also describe the influence of near-interface defects in the oxides (border traps) and why these particular defects are so significant for arsenide MOS devices. An attempt will be made to associate electrically-active traps detected at different energies in the III-V semiconductor bandgap with specific surface and point defects, based on prior reported experimental and computational observations. The difficulty of quantifying trap densities using typical capacitance-voltage and conductance-voltage methods developed for silicon MOS will be discussed.

<sup>1</sup>Support by the SRC Non-Classical CMOS Center is gratefully acknowledged.