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QM/EM simulation of Junctionless FinFET JIE PENG, LINYI MENG, CHIYUNG YAM, GUANHUA CHEN, Department of Chemistry,University of Hong Kong, Hong Kong, China — We present here the simulations of a junctionless transistor. Its source, channel and drain are embeded in a piece of uniformly doped silicon nanowire. In the earlier stage, it has been designed to be a normally "ON" device. Quite reversely, the first experimentally presented junctionless transistor is in the "OFF" state when the applied gate voltage is absent. Simulations show that the depletion occurs between the nanowire and hetero-doped gate. A "P-N junction" is formed in the junctionless transistor, whose direction is perpendicular to the direction of the current flowing. Our simulation considers the depletion effect in the Qauntum mechanical calculation. I-V curves of transistors with the gate doped by the same and different type of dopants have been obtained. The results match the experiments.

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