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Fabrication, electrical characterization and scanning gate microscopy of Schottky silicon nanowire devices SORIN MELINTE, ANDRA IORDANESCU, CONSTANTIN DUTU, DENIS FLANDRE, ELEN/ICTM, Universite catholique de Louvain, Belgium, SEBASTIEN FANIEL, FREDERICO MARTINS, BENOIT HACKENS, NAPS/IMCN, Universite catholique de Louvain, Belgium, ICTM TEAM, IMCN TEAM — We report the fabrication and the electrical characterization of Schottky silicon nanowire field effect transistors. Our devices are built with a top down approach on silicon-on-insulator wafers with (100) crystallographic orientation and 10 - 25 Ω.cm resistivity of the silicon top layer. The transistor's channel is assured by silicon nanowires patterned by electron beam lithography and wet etching. The nanowires have nominal cross sections down to 30×30 nm^2. For example, platinum-silicon Schottky contacts are made by physical deposition of a platinum layer followed by an annealing at 500°C for 2 minutes in a N_2 atmosphere. The devices are characterized at various temperatures by current-voltage measurements and scanning gate microscopy techniques. Varying the dimensionality and geometry of the contacts, the nature of metal-semiconductor junctions and the substrate strain, we get new insights into the influence of trapped charges at the $Si - SiO_2$ interface on transport through SiO_2-enclosed nanowires, at the nanometer scale.

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