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Electrical Properties of p-Ge and p-GeSn materials grown on n-Si substrates THOMAS R. HARRIS, YUNG KEE YEO, Department of Engineering Physics, Air Force Institute of Technology, Wright-Patterson AFB, OH 45433-7765, USA, MEE-YI RYU, Department of Physics, Kangwon National University, Kangwon-Do 200-701, Korea, RICHARD BEELER, JOHN KOUVETAKIS, Department of Chemistry and Biochemistry, Arizona State University, Tempe, Arizona 85287-1504, USA — The electrical properties of *p*-Ge and *p*-Ge_{1-*y*}Sn_{*y*} (*y*=0.06-0.1%) grown on *n*-Si substrate were investigated through temperature-dependent Hall-effect measurements. It was found that there exists a degenerate parallel conducting layer in Ge_{1-*y*}Sn_{*y*}/Si as well as a second, deeper acceptor in addition to a shallow acceptor. Additionally, a conductivity type conversion from *p* to *n* was observed between 370 and 440 K for these samples. The parallel conducting layer dominates the electrical properties of the Ge_{1-*y*}Sn_{*y*} layer below 50 K, and also significantly affects those properties at higher temperatures. The conductivity type conversion and causes of the degenerate conduction layer will be discussed.

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