Abstract Submitted
for the MAR13 Meeting of
The American Physical Society

Integration of on-chip FET switches with dopantless Si/SiGe quantum dot structures for high throughput testing DANIEL WARD, DONALD SAVAGE, MAX LAGALLY, SUSAN COPPERSMITH, MARK ERIKSSON, University of Wisconsin-Madison — In the last few years, significant research on dopantless Si/SiGe planar quantum dot structures has occurred. One of the limiting factors is that typically only a single double-dot structure can be cooled down in a dilution refrigerator at time due to the limited number of electrical connections available. We report on our recent work to create samples with four sets of double-dots on a single chip that can all be tested in a single cool down through the introduction of on-chip FET switches. In our samples the four double-dot structures have their depletion gates and ohmic contacts connected in parallel, minimizing the number of connections. We energize accumulation gates for the device under test such that the other dot structures do not contribute to the measurements. Our double-dot structures require five accumulation gates, which limits scaling due to limited fridge wiring capacity. To alleviate this problem and to test integration approaches for cryogenic quantum dot devices we fabricated a series of on-chip FET switches to form a multiplexer for the accumulation gates. Using the multiplexer we can wire up four double-dot structures using just 23 connections instead of the 34 required without it. As more devices are added the scaling benefits increase exponentially.

Daniel Ward
University of Wisconsin-Madison

Date submitted: 09 Nov 2012 Electronic form version 1.4