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Characterization of Silicon CMOS Quantum Well Field Effect Transistors CLINT NAQUIN, MARK LEE, University of Texas at Dallas, HAL EDWARDS, TATHAGATA CHATTERJEE, Texas Instruments — Silicon CMOS field effect transistors (FETs) incorporating quantum wells (QWs) are of potential interest as advanced oscillators and sensors. We report on the design and electrical characterization of a set of Si CMOS QW FETs fabricated using industrial 45 nm processing. By using low doped drain and pocket implants, lateral QW potentials between 30 nm to 100 nm in length and approximately 0.1 to 0.5 eV in potential depth have been incorporated into the channel between source and drain. The potential depth can be modulated by the gate voltage. Measurements of drain current as a function of gate voltage for devices from 1.7 K up to room temperature will be reported, with the expectation of observing resonant conductance oscillations from transport through QW levels at temperatures where the QW energy levels are well formed.

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