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Elucidating Bias Stress in Vertical and Lateral Charge Transport in Organic Electronics HE WANG, Princeton University, CHERNO JAYE, ZUGEN FU, DANIEL FISCHER, National Institute of Standards and Technology, YUEH-LIN LOO, Princeton University — Bias stress, during which a reduction in source-drain current is observed under continuous application of gate voltage in organic thin-film transistors, originates from trapped mobile charges. Organic semiconductors often exhibit tail states that extend into their band gap; these tail states can act as traps to immobilize charge. Alternatively, defects at the organic semiconductor-dielectric interface can also trap charge. Whether bias stress originates from impurities or defects in the bulk of the organic semiconductor or at the organic semiconductor-dielectric interface, however, remains unclear. By building and testing organic single-carrier diodes having different active layer thicknesses, we can infer the trapping contributions in the bulk of the organic semiconductor relative to those at the organic semiconductor-electrode interface. In conjunction with device characteristics of organic thin-film transistors having different dielectrics, we found that the broad distribution of tail states that is present in poly(3-hexyl thiophene), P3HT, is responsible for bias stress in P3HT-comprising devices. On the other hand, traps at the [6,6]-phenyl-C61-butyric acid methyl ester, PCBM,-dielectric interface are more dominant than those in the bulk in PCBM-containing devices.

He Wang
Princeton University

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