Abstract Submitted
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Thermoelectric properties of electrolessly etched silicon nanowire arrays JYOTHI SADHU, HONGXIANG TIAN, JUN MA, KRISHNA VALAVALA, PIYUSH SINGH, SANJIV SINHA, Dept of Mechanical Science and Engg, Urbana — Patterning silicon as nanowires with roughened sidewalls enhances the thermoelectric figure-of-merit ZT by order of magnitude compared to the bulk at 300 K [1]. The enhancement is mainly achieved by the remarkable reduction in the thermal conductivity below 5 W/mK at 300 K with only a negligible effect on the power factor of these nanowires. While the focus remained on understanding the implications of surface disorder on the thermal conductivity, the phonon transport effects on the Seebeck coefficient of these wires remains largely unexplored. We developed an electroless etching technique to generate nanowire arrays (NWAs) with controlled surface roughness, morphology, porosity and doping [2]. We conduct the simultaneous device-level measurements of the Seebeck coefficient and thermal conductivity of the NWAs using frequency domain techniques. We observe that nano-structuring quenches the phonon drag [3] in NWAs thereby reducing the Seebeck coefficient by $\sim$25% compared to the bulk at degenerate doping levels. Further, we observe that the sidewall roughness greater than 3 nm roughness height lowers the thermal conductivity 75% below the Casimir limit [4] with 10% - 15% increase in Seebeck coefficient. The porous NWAs show thermal conductivity close to the amorphous limit of Si with enhancement in the Seebeck coefficient primarily due to the carrier depletion. References: [1] A. I. Hochbaum et al, Nature 451, 163-167 (2008). [2] K. Balasundaram et. al., Nanotechnology 23, 305304 (2012). [3] C. Herring, Phys. Rev. 96, 1163 (1954). [4] H. G. B. Casimir, Physica 5, 495 (1938).

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