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Role of defects in resistive switching TiO_2- and $SrTiO_3$-based devices

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Oxide-based resistive switching devices hold promise of being the next generation of non-volatile high density memory. While small size, fast switching and long retention time have been demonstrated, many questions remain pertaining the switching mechanism. In particular, the role of point and extended defects in resistance switching remains to be elucidated. Most proposed interpretations invoke oxygen vacancy redistribution as the origin of the resistance change. However, the measurements of the vacancy drift in the Schottky barriers on $SrTiO_3$ indicated that mobility at room temperature is eight orders of magnitude too low to account for the reported switching times. This difficulty could be alleviated by faster vacancy motion along the dislocation lines and/or local Joule heating during switching. Careful mapping of the dislocation distribution before and after switching in nanoscale devices did not find a good correlation between dislocations and the I-V characteristics. Lateral $SrTiO_3$ devices with no dislocations have similar switching behavior to the ones fabricated on high dislocation density materials. The only correlation present was the generation of dislocations in devices with dissipated power level above 10 mW. The apparent mechanism is the thermal stress driven plastic deformation. While the Joule heating could speed up the defect motion, it could not explain the long retention times. This is frequently interpreted as due to formation of oxygen-deficient phases in TiO_2-based memristors. Transmission Electron Microscopy analysis of nanoscale vertical devices has revealed numerous physical changes with the extent strongly dependent on the level of dissipated power. Optimized device structures that switch with the power dissipation below 2 mW exhibited very limited degree of crystallization and no new phases. Many of the initially posed questions remain unanswered.