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Topological Properties of Combinational Logic Functions for Very Large Scale Integrated Circuits ELIZABETH HITESHUE, University of Pennsylvania, KELSEY IRVIN, Washington University in St. Louis, MARY LANZEROTTI, Air Force Inst of Tech - WPAFB, GRAZIANO VERNIZZI, JOSEPH KUJAWSKI, ALLAN WEATHERWAX, Siena College — This talk presents topological properties of combinational logic functions implemented with basic logic gates. Combinational logic can be implemented in very large scale integrated circuits, including high-performance microprocessors. Prior work has produced an historically-equivalent (HE) interpretation of Mr. E. F. Rent's 1960 memos for today's complex circuitry, an application to modern microprocessors [1-5], and topological constraints for electronic circuits [6]. This talk will examine combinational logic blocks which may exhibit different connectivity and will evaluate their topological properties.

References: [1] B. Landman and R.Russo, IEEE Trans. Comput., vol. C-20, pp. 1469-1478, 1971; [2] M. Lanzerotti, G. Fiorenza, R. Rand, IBM Jnl. Res. and Develop., vol. 49, pp. 777-803, 2005; [3] M. Lanzerotti, G. Fiorenza, and R. Rand, IEEE Trans. VLSI Syst., vol. 12, pp. 1330-1347, 2004; [4] D. Stroobandt, IEEE Solid-State Circuits Mag., vol. 2, issue 1, pp. 21-27, 2010; [5] M. Lanzerotti, G. Fiorenza, R. Rand, 2011 Proc. APS March Mtg, Dallas, TX, 2011; [6] G. Vernizzi, M. Lanzerotti, J. Kujawski, A. Weatherwax, "Topological Constraints for E. F. Rent's Work on Microminiature Packaging and Circuitry," IBM Jnl. Res. and Dev., in press.

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