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Wafer-scale integration of graphene heterojunction transistors for low-power electronics JINSEONG HEO, KYUNG-EUN BYUN, JAEHO LEE, HYUN-JONG CHUNG, SANGHUN JEON, SEONGJUN PARK, SUNGWOO HWANG, Samsung Advanced Institute of Technology — Recently, vertical graphene field effect transistors (VGFETs) in which graphene is combined with semiconductors including layered two-dimensional materials have attracted much attention for application in digital electronics. Work-function tunability of graphene was employed in VGFETs to modulate energy barrier between graphene and semiconductors, and therefore Ion/Ioff was dramatically increased. Here, we demonstrate wafer-scale VGFETs based on graphene-thin semiconductor-metal asymmetric junctions on a transparent 150 $\times$ 150 mm2 glass. In this system, a triangular energy barrier between the graphene and metal is designed by selecting a metal with a proper work function. We obtain a maximum Ion/Ioff up to 1,000,000 with an average of 3,010 over 2,000 devices at ambient conditions. Furthermore, an inverter that combines complementary n-type and p-type devices was demonstrated to operate at a bias of only 0.5 V.

Jinseong Heo
Samsung Advanced Institute of Technology

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