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**Ferroelectric Superlattices as a route to clean Graphene-ferroelectric Interfaces**[1] MOHAMMED YUSUF, MATTHEW DAWBER, XU DU, SUNY Stony Brook — A good interface between ferroelectric surfaces and graphene sheets can enable a new generation of multifunctional devices in which the ferroelectric material is used to control the properties of graphene. Ferroelectric superlattices, in particular $PbTiO_3/SrTiO_3$ (PTO/STO), provide us with a unique opportunity for studying the graphene-ferroelectric interface. The ferroelectric-paraelectric transition temperature of the superlattices is tunable by varying the PTO volume fraction. Using devices with different PTO volume fractions and different ferroelectric strength, we have successfully demonstrated ferroelectric hysteresis, charge-trapping associated anti-hysteresis, and cross-over from anti-hysteresis to hysteresis over a wide temperature range from 300K down to 4K. These results allow us to establish a deeper understanding of the graphene-ferroelectric interface. Contrary to the common understandings that the charge trapping centers and anti-hysteresis originate mainly from contaminants and adsorbates trapped between graphene and ferroelectric substrates during fabrication, we found that significant contribution of charge trapping may come from defects in the ferroelectric substrate itself, and we explore approaches to eliminating these.

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Mohammed Yusuf
SUNY Stony Brook

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