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High-Performance Gate Dielectric for Carbon-based Nanoelectronics

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Gate dielectric layer with high-quality and high-efficiency is an important component and technological challenge for high-performance top-gated carbon-based field-effected transistors (FETs) including carbon nanotube (CNT) FETs and graphene FETs. We address high-quality yttrium oxide (Y_2O_3), which can be grown on CNT/graphene through a simple and cheap process. Top-gate CNT FETs adopting 5 nm Y_2O_3 layer as its gate dielectric showed excellent device characteristics, especially including an ideal subthreshold swing of 60 mV/decade (up to the theoretical limit of an ideal FET at room temperature). High quality Y_2O_3 dielectric layer has also been integrated into top-gate G-FETs as gate insulator layer, and its thickness has been reduced continuously down to 3.9 nm with an equivalent oxide thickness (EOT) of 1.5 nm and excellent insulativity. High carrier mobility up to 5400 cm2/V·s and high top gate efficiency of up to 120 (relative to that of back gate with 285 nm SiO_2) are simultaneously realized in G-FETs with high quality Y_2O_3 gate oxide at high oxidizing temperature. Moreover, benefitted from large gate capacitance as 2.28 μF/cm2, quantum capacitance in graphene has been accurately measured and retrieved.