Abstract Submitted
for the MAR14 Meeting of
The American Physical Society

Towards Multiple-Bit-Per-Cell Operation In a Single Active Layer-Phase Change Memory Cell[1] IBRAHIM CINAR, VEDAT KARAKAS, ONUR DINCER, OZGUR BURAK ASLAN, AISHA GOKCE, Bogazici University, Department of Physics Bebek, 34342 Istanbul, Turkey, BARRY STIPE, JORDAN A. KATINE, HGST, A Western Digital Company, 95135 San Jose, California, USA, GULEN AKTAS, OZHAN OZATAY, Bogazici University, Department of Physics Bebek, 34342 Istanbul, Turkey — High contrast between 0 and 1 logic states in addition to other superior properties of phase change memory (PCM) brought out the possible application of multiple logic levels in a single bit in an effort to boost data storage density. The potential stabilization of resistance levels in between the 0 polycrystalline and 1 amorphous states enables storage of several data in a single device cell (such as 00, 01,10,11 levels). Here we report our investigation of the role of contact geometry and fabrication induced modification of phase change kinetics in stabilizing mixed phase states in an effort to obtain such multiple-bit per cell operation within a single layer PCM material system ($Ge_2Sb_2Te_5$). The nature of switching dynamics appears highly sensitive to exact programming current distribution and defect density such that a nanoscale square contact with effective current localization at the sharp corners facilitates the formation of stable intermediate phases as compared to a circular one. Resistance maps show that the top contact geometry and engineering of defects can be used as an effective handle to tune the resistance states to optimize memory cells for ultra-high density storage.

[1]This work has been supported by the European Commission FP7 Marie Curie IRG grant: PCM-256281

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Date submitted: 15 Nov 2013 Electronic form version 1.4