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Negative Differential Transconductance in Silicon CMOS Quantum Well Field Effect Transistors CLINT NAQUIN, MARK LEE, University of Texas at Dallas, HAL EDWARDS, TATHAGATA CHATTERJEE, GURU MATHUR, Texas Instruments — Quantum well (QW) devices are potentially useful as high-speed oscillators and sensors, as well as high-density memory and multi-state logic. Historically, these devices have been built using III-V heterostructures grown epitaxially in the vertical direction. Silicon CMOS field effect transistors (FETs) that incorporate QWs through the lateral confinement of a silicon inversion layer are of particular interest due to their capability for mass production and industrial scalability. We report on the observation of negative differential transconductance (NDTC) in a set of Si CMOS QW FETs fabricated using industrial 45 nm node processing. Measurements of drain current as a function of gate voltage from 5 K to room temperature were conducted, and local current maxima and minima were observed leading to negative differential transconductance. When voltage-biasing the body terminal, NDTC appears at temperatures as high as 218 K; however, for measurements taken with the body terminal current-biased, NDTC appears at higher temperatures with peak-to-valley ratios (PVR) greater than two.

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